IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/137,584, filed May 2, 2002, ~~pending~~ now U.S. Patent 6,583,503, issued June 24, 2003, which is a continuation of application Serial No. 09/834,706, filed April 13, 2001, now U.S. Patent ~~6,404,044 B2~~ 6,404,044, issued June 11, 2002, which is a continuation of application Serial No. 09/466,454, filed December 17, 1999, now U.S. Patent 6,222,265, issued April 24, 2001, which is a continuation of application Serial No. 09/233,997, filed January 19, 1999, now U.S. Patent 6,051,878, issued April 18, 2000, which is a divisional of application Serial No. 08/813,467, filed March 10, 1997, now U.S. Patent 5,994,166, issued November 30, 1999.

Please replace paragraph number **[0002]** with the following rewritten paragraph:

[0002] Field of the Invention: The present invention relates to an apparatus and a method for increasing semiconductor device density. In particular, the present invention relates to a stacked multi-substrate device using a combination of flip chips and ~~chip-on-~~chip-on-board assembly techniques to achieve densely packaged semiconductor devices.

Please replace paragraph number **[0003]** with the following rewritten paragraph:

[0003] State of the Art: Chip-On-Board techniques are used to attach semiconductor dice to a printed circuit board, including ~~flip-~~flip-chip attachment, wirebonding, and tape automated bonding ("TAB"). ~~Flip-~~Flip-chip attachment consists of attaching a flip chip to a printed circuit board or other substrate. A flip chip is a semiconductor chip that has a pattern or array of electrical terminations or bond pads spaced around an active surface of the flip chip for face down mounting of the flip chip to a substrate. Generally, the flip chip has an active surface having one of the following electrical connectors: Ball Grid Array ("BGA") - wherein an array of minute solder balls is disposed on the surface of a flip chip that attaches to the substrate ("the attachment surface"); Slightly Larger than Integrated Circuit Carrier ("SLICC") - which is similar

to a BGA, but having a smaller solder ball pitch and diameter than a BGA; or a Pin Grid Array ("PGA") - wherein an array of small pins extends substantially perpendicularly from the attachment surface of a flip chip. The pins conform to a specific arrangement on a printed circuit board or other substrate for attachment thereto. With the BGA or SLICC, the solder or other conductive ball arrangement on the flip chip must be a mirror-image of the connecting bond pads on the printed circuit board such that precise connection is made. The flip chip is bonded to the printed circuit board by refluxing the solder balls. The solder balls may also be replaced with a conductive polymer. With the PGA, the pin arrangement of the flip chip must be a mirror-image of the pin recesses on the printed circuit board. After insertion, the flip chip is generally bonded by soldering the pins into place. An under-fill encapsulant is generally disposed between the flip chip and the printed circuit board for environmental protection and to enhance the attachment of the flip chip to the printed circuit board. A variation of the pin-in-recess PGA is a J-lead PGA, wherein the loops of the J's are soldered to pads on the surface of the circuit board.

Please replace paragraph number **[0011]** with the following rewritten paragraph:

[0011] U.S. Patent 5,434,745, issued ~~July,~~ July 18, 1995 to Shokrgozar et al. ("Shokrgozar"), discloses a stackable packaging module comprising a standard die attached to a substrate with a spacer frame placed on the substrate to surround the die. The substrate/die/spacer combinations are stacked one atop another to form a stacked assembly. The outer edge of the spacer frame has grooves in which a conductive epoxy is disposed. The conductive epoxy forms electric communication between the stacked layers and/or to the final substrate to which the stacked assembly is attached. However, Shokrgozar requires specialized spacer frames and a substantial number of assembly steps, both of which increase the cost of the final assembly.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] U.S. Patent 5,513,076, issued April 30, 1996 to ~~Wether~~ Werther ("~~Wether~~Werther"), teaches the use of interconnecting assemblies to connect integrated circuits in an integrated manner.

Please replace paragraph number **[0016]** with the following rewritten paragraph:

[0016] The present invention relates to a stacked multi-substrate device using combined flip chips and chip-on-board assembly techniques to achieve densely packaged semiconductor devices, and a method for making same. In this invention, multiple substrates are stacked atop one another. The substrates can include a plurality of semiconductor dice disposed on either surface of the substrates. The substrates can be structures of planar ~~non-~~non-conductive material, such as fiberglass material used for PCBs, or may even be semiconductor dice. For the sake of clarity, the term "substrate," as used hereinafter, will be defined to include planar non-conductive materials and semiconductor dice. The substrates are preferably stacked atop one another by electric connections which are ball or column-like structures. Alternately, solder bumps or balls may be formed on the substrate. The electric connections achieve electric communication between the stacked substrates. The electric connections can be formed from industry standard solder forming techniques or from other known materials and techniques, such as conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, TAB tape, and the like. The electric connections must be of sufficient height to give clearance for the components mounted on the substrates and should be sufficiently strong enough to give support between the stacked substrates.

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] A preferred embodiment comprises a base substrate, having first and opposing surfaces, and means for electrical connection with external components or substrates, wherein the electrical connection means extends at least from the first surface of the base substrate. The base substrate opposing surface, the other side of the substrate, also includes a plurality of bond pads

disposed thereon. Additionally, at least one semiconductor component may be attached to the opposing surface of the base substrate. The semiconductor components are preferably flip chips that are in electrical communication with electrical traces on or within the base substrate with any convenient known chip-on-board (COB) or direct-chip-attachment (DCA) technique (i.e., ~~flip~~ flip-chip attachment, wirebonding, and TAB). Other techniques, such as the use of two-axis materials or conductive epoxies, can also be used for connections between either substrates or substrates and semiconductor chips. The electrical traces form a network of predetermined electrical connections between the base substrate electrical connection means, the base substrate bond pads, and/or the base substrate semiconductor components.

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] FIG. 6 is a cross-sectional view of a variable stack size assembly of the present invention using ~~flip~~ flip-chip bonding techniques.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] FIG. 1 illustrates a first stacked assembly 100 of the present invention. The stacked assembly 100 comprises a base substrate 102 having a first surface 104 with a plurality of bond pads 106 disposed thereon and a second surface 108 with a plurality of bond pads 110 disposed thereon. Each of the base substrate first surface bond pads 106 is in electrical communication with its respective base substrate second surface bond ~~pads~~ pad 110 via a plurality of lead traces 112 extending through the base substrate 102. A plurality of electric connections 114 extends from the base substrate first surface bond pads 106. The base substrate electric connections 114 make contact with the other components or substrates.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] A plurality of second semiconductor dice 150 each having a face side 152 and a back side 154 is attached to the second stacked substrate first surface 142 with a second layer of adhesive 156 applied to the second semiconductor die back sides 154. The second

semiconductor dice 150 are in electrical contact with a plurality of second stacked substrate electrical traces 158 via wirebonds 160. A plurality of third semiconductor dice 162 each having a face side 164 is attached to the second stacked substrate second surface 146 with a plurality of ~~flip-~~flip-chip contacts 166, such as BGA, PGA or the like. The ~~flip-~~flip-chip contacts 166 are in electrical contact with the second stacked substrate electrical traces 158. The second stacked substrate electrical traces 158 extend in or on the second stacked substrate 140 and may contact the second stacked substrate first surface bond pads 144, the second semiconductor dice 150 and/or another third semiconductor die 162.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] A ~~flip-~~flip-chip dielectric material 168 may be disposed between the third semiconductor dice face side 164 and the second stacked substrate second surface 146. Additionally, a dielectric material 170 may be disposed between the base substrate 102 and the first stacked substrate 116, and/or the first stacked substrate 116 and the second ~~stack~~ stacked substrate 140. Furthermore, an encapsulation material 172 may cover the ~~stack~~ stacked dice portion of the stacked assembly 100.

Please replace paragraph number **[0047]** with the following rewritten paragraph:

[0047] FIG. 5 illustrates a substrate assembly 600 having a smaller substrate 602 on a larger substrate 604, such as shown as third stacked substrate 462 and second small stacked substrate 494 in FIG. 4. The substrate assembly 600 comprises the larger substrate 604 having a plurality of first semiconductor dice 606 and the smaller substrate 602 disposed on a surface 608 of the larger substrate 604. The first semiconductor dice 606 have a face side 612 and a back side 614. The first semiconductor dice 606 are attached by a first layer of adhesive 616 applied to the semiconductor dice back side 614 and make electrical contact with the substrate surface 608 by a plurality of first bond wires 618. The smaller substrate 602 has a first surface 620 and a second surface 622. The smaller substrate 602 has a plurality of electrical contacts 624 extending between a plurality of bond pads 626 on the smaller substrate first

surface 620 and a plurality of bond pads 628 on the larger substrate surface 608. A plurality of second semiconductor dice 630 (only one shown) is disposed on the smaller substrate second surface 622. The second semiconductor dice 630 have a face side 634 and a back side 636. The second semiconductor dice 630 are attached by a second layer of adhesive 638 applied to the second semiconductor dice back side 636 and ~~make~~ makes electrical contact with the smaller substrate second surface 622 by a plurality of bond wires 640. Although the electrical traces of the smaller substrate have not been illustrated, it is understood that electrical traces make electrical connections in the same manner as described for FIG. 1.

Please replace paragraph number **[0048]** with the following rewritten paragraph:

[0048] FIG. 6 illustrates a substrate assembly 700 having a plurality of semiconductor devices mounted on substrates using known ~~flip~~-flip-chip attachment techniques. The substrate assembly 700 comprises a first substrate 704 having a plurality of first semiconductor dice 702 disposed thereon and a second substrate 708 having a plurality of second semiconductor dice 706 disposed thereon. The first semiconductor dice 702 each have a surface or face side 710 having a plurality of bond pads (not shown) thereon and a back side 712. The first semiconductor dice 702 make electrical contact with the traces (not shown) on the first substrate surface 714 by a plurality of first conductive material balls 716 extending between the bond pads (not shown) on the face surface 710 of the dice 702 and the traces (not shown) on the first substrate surface 714. The balls 716 may be made of any suitable conductive material to connect the semiconductor dice 702 to the conductive traces on first substrate 704, such as solder, conductive epoxy, etc. The balls 716 are shown as generally spherical in shape, although they may be any suitable geometric shape and size for bonding purposes. Further, z-axis connectors may be substituted for the balls 716 if so desired. The second substrate 708 has a surface 718 having a plurality of conductive traces (not shown) thereon. The second plurality of semiconductor dice 706 each have a face side 720 having a plurality of bond pads (not shown) thereon and a back side 722. The second plurality of semiconductor dice 706 make electrical contact with the second substrate surface 718 by a plurality of second conductive material balls 724 extending between the bond

pads of the dice 706 and the conductive traces on the second substrate surface 718. The balls 724 may be made of any suitable conductive material to connect the semiconductor dice 706 to the conductive traces on second substrate 708, such as solder, conductive epoxy, etc. The balls 724 are shown as generally spherical in shape, although they may be any suitable geometric shape and size for bonding purposes. Further, z-axis connectors may be substituted for balls 724 if so desired. The desired conductive traces on the surface 714 of the first substrate 704 are connected to the desired conductive traces on the surface 718 of the second substrate 708 by larger conductive balls 726. The larger conductive balls 726 may be of any suitable conductive material, such as solder, conductive epoxy, etc. The larger conductive balls are also used for connecting the surface 728 of the first substrate 704 to any other desired substrate. Further, z-axis connectors may be substituted for balls 726 if so desired. It should be understood that the conductive traces which have only been referred to on the surfaces 714 and 718 of the substrates may be formed on either side of the first substrate 704 or the second substrate 708 and, as such, have not been illustrated. Also, any connectors extending through the first substrate 704 and second substrate 708 for connection purposes have not been shown. Similarly, the bond pads on the first semiconductor dice 702 and second semiconductor dice 706 have not been illustrated. The first semiconductor dice 702 are attached to the first substrate 704 and the second semiconductor dice 706 are attached to the second substrate 708 by well known flip chip bonding techniques, depending upon the type of conductive balls 716 and 724 used for connection purposes.